REMARKS

Claims 1 and 2 remain in the application and claim 1 has been amended hereby. Claims 3-20 have been cancelled and claims 21 and 22 have been added.

Reconsideration is respectfully requested of the rejection of claims 1-20 under 35 USC 112, second paragraph, as being indefinite.

Claims 3-20 have been cancelled, thereby rendering the rejection thereof moot.

Claim 1 has been amended in part to clarify that the data is the real-time audiovisual data transmitted by the second digital signal processing apparatus, as requested in the Office Action at paragraph 4.

Accordingly, it is respectfully submitted that amended independent claim 1, and claim 2 depending therefrom, are clear and definite in their recitation of the present invention and meet all requirements of 35 USC 112.

Reconsideration is respectfully requested of the rejection of claims 1, 3-5, 7, 9-11, 13-15, 17, 19, and 20 under 35 USC 102(e), as being anticipated by Rosefield et al.

Features of the presently claimed invention are a predetermined digital bus that supports real-time audiovisual data transmission and asynchronous control data transmission and has a plurality of electronic apparatuses connected thereto.

Looking at the bus in Rosefield et al. we see that it is a sample rate converter (SRC) bus using buffer memories so it cannot support real-time data transmission. See also the set

of buffers 38 in Fig. 1 of Rosefield et al.

Further, looking at Rosefield et al. we see that the plurality of electronic apparatuses are connected via a PCI bus to the first DSP and not to the predetermined digital bus such as in the presently claimed invention. See Fig. 1 of Rosefield et al.

Other features of the presently claimed invention are a first digital signal processing apparatus including real-time data receiving means for receiving real-time audiovisual data transmitted from a second digital signal processing apparatus. Looking at Rosefield et al. we see that the first DSP (34) is not receiving real-time audiovisual data transmitted from the second DSP (36) but it is the second DSP (36) that is receiving input data streams from the first DSP (34) through buffers of the SRC interface. See col. 3, line 67 to col. 4, line 3 of Rosefield et al.

Accordingly, at least for the above-discussed reasons, it is respectfully submitted that amended independent claim 1, and claim 2 depending therefrom, are not anticipated by Rosefield et al.

Reconsideration is respectfully requested of the rejection of claims 2, 6, 8, 12, 16, and 18 under 35 USC 103(a), as being unpatentable over Rosefield et al. in view of Lin.

Claims 6, 8, 12, 16 and 18 have been cancelled, thereby rendering the rejection thereof moot.

Claim 2 depends from claim 1, which for the reasons stated above it is submitted to be patentably distinct over

Rosefield et al. and, because there are no features in Lin that somehow could be combined with Rosefield et al. and result in the presently claimed invention, it is respectfully submitted that claim 2 is patentably distinct over Rosefield et al. in view of Lin.

Entry of this amendment is earnestly solicited, and it is respectfully submitted that the amendments made to the claims hereby raise no new issues requiring further consideration and/or search, because all of the features of this invention have clearly been considered by the examiner in the prosecution of this application and because the present amendments serve only to further define and emphasize the novel features of this invention.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,
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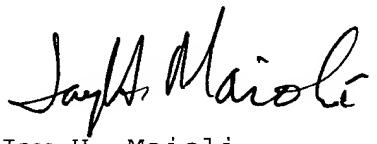

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